CLAIMS:

What is claimed is:

1. A method in a data processing system for processing instructions, the method comprising:

responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether the instruction indicates enabling a mode of operation in which interrupts are to be generated;

responsive to receiving a subsequent instruction after receiving the instruction, determining whether the instruction is of a certain type; and

generating an interrupt if the mode of operation in which interrupts are to be enabled and the instruction is of the certain type.

2. The method of claim 1 further comprising:

responsive to receiving a subsequent instruction in the subsequent instructions indicating disablement of the mode of operation in which interrupts are to be generated, disabling the mode of operation in which interrupts are to be generated.

3. The method of claim 1, wherein the generating step comprises:

sending a signal from an instruction cache to an interrupt unit in the processor; and

processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

4. The method of claim 3, wherein the processing step includes:

executing code associated with the interrupt.

5. The method of claim 4, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.

6. The method of claim 4, wherein the code counts a number of times the instruction of the certain type has been executed.

7. The method of claim 1, wherein the instruction is received in a bundle and wherein the indicator comprises at least one spare bit in a field in the bundle.

8. The method of claim 1, wherein the instruction of the certain type is a branch instruction.

9. A data processing system comprising:

an interrupt unit, wherein the interrupt executes code in response to receiving a signal is received; and

an instruction cache, wherein the instruction cache receives instructions and sends the signal to the interrupt unit if a mode of operation to generate interrupts is enabled and an instruction of a certain type is received for execution by the instruction cache.

10. A data processing system for processing instructions, the data processing system comprising:

first determining means, responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, for determining whether the instruction indicates enabling a mode of operation in which interrupts are to be generated;

second determining means, responsive to receiving a subsequent instruction after receiving the instruction, determining whether the instruction is of a certain type; and

generating means for generating an interrupt if the mode of operation in which interrupts are to be enabled and the instruction is of the certain type.

11. The data processing system of claim 10 further comprising:

disabling means, responsive to receiving a subsequent instruction in the subsequent instructions indicating disablement of the mode of operation in which interrupts are to be generated, for disabling the mode of operation in which interrupts are to be generated.

12. The data processing system of claim 10, wherein the generating means comprises:

sending means for sending a signal from an instruction cache to an interrupt unit in the processor; and

processing means for processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

13. The data processing system of claim 12, wherein the processing means includes:

executing means for executing code associated with the interrupt.

14. The data processing system of claim 13, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.

15. The data processing system of claim 13, wherein the code counts a number of times the instruction of the certain type has been executed.

16. The data processing system of claim 10, wherein the instruction is received in a bundle and wherein the indicator comprises at least one spare bit in a field in the bundle.

17. The data processing system of claim 10, wherein the instruction of the certain type is a branch instruction.

18. A computer program product in a computer readable medium for processing instructions, the computer program product comprising:

first instructions, responsive to receiving an instruction for execution in an instruction cache in a

processor in the data processing system, for determining whether the instruction indicates enabling a mode of operation in which interrupts are to be generated;

second instructions, responsive to receiving a subsequent instruction after receiving the instruction, for determining whether the instruction is of a certain type; and

third instructions, for generating an interrupt if the mode of operation in which interrupts are to be enabled and the instruction is of the certain type.

19. The computer program product of claim 18 further comprising:

fourth instructions, responsive to receiving a subsequent instruction in the subsequent instructions indicating disablement of the mode of operation in which interrupts are to be generated, for disabling the mode of operation in which interrupts are to be generated.

20. The computer program product of claim 18, wherein the third instructions comprises:

first sub-instructions for sending a signal from an instruction cache to an interrupt unit in the processor; and

second sub-instructions for processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

21. The computer program product of claim 20, wherein the second sub-instructions includes:

instructions for executing code associated with the interrupt.

22. The computer program product of claim 21, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.